



U.S.S.N. 10/828,542  
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Supplemental Response to Office Action

## LISTING OF THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in this application. Added text is indicated by underlining, and deleted text is indicated by ~~strikethrough~~. Changes are identified by a vertical bar in the margin.

Please cancel Claims 1-4.

5. (Currently amended) A cluster resonator, comprising:  
a first conducting plane;  
a second substantially parallel conducting plane;  
a cluster of vias of essentially uniform length oriented substantially  
normal to the conducting planes, each via in the cluster comprising a first end  
and a second end;  
a first conducting pad disposed in a third plane substantially parallel  
and capacitively coupled to the first conducting plane and physically coupled  
with the vias of the cluster of vias proximate their first ends; and  
a second conducting pad disposed in a fourth plane substantially  
parallel and capacitively coupled to the second conducting plane and  
physically coupled with the vias of the cluster of vias proximate their second  
ends, wherein the vias are physically connected to only the first and second  
conducting pads; and  
wherein a combined inductance and capacitance of the cluster of vias  
form an electromagnetically resonant shunt circuit between the first and  
second conducting planes; and

wherein the vias of the cluster of vias are disposed along a perimeter that defines an interior region and one or more interior vias are routed within the interior region of the cluster of vias; and

~~The cluster resonator of claim 4,~~ wherein the interior vias comprise portions of transmission lines passing electrical signals through the cluster resonator.

6. (Currently amended) A cluster resonator, comprising:  
a first conducting plane;  
a second substantially parallel conducting plane;  
a cluster of vias of essentially uniform length oriented substantially normal to the conducting planes, each via in the cluster comprising a first end and a second end;  
a first conducting pad disposed in a third plane substantially parallel and capacitively coupled to the first conducting plane and physically coupled with the vias of the cluster of vias proximate their first ends; and  
a second conducting pad disposed in a fourth plane substantially parallel and capacitively coupled to the second conducting plane and physically coupled with the vias of the cluster of vias proximate their second ends, wherein the vias are physically connected to only the first and second conducting pads; and

~~The cluster resonator of claim 1,~~ wherein the first or second conducting pad is external relative to the first and second conducting planes.

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7. (Currently amended) The cluster resonator of claim 45, wherein the first or second conducting pad is internal relative to the first and second conducting planes.

8. (Canceled)

9. (Canceled)

10. (Currently amended) The cluster resonator of claim 45, wherein the first and second conducting pads are internal relative to the first and second conducting planes.

11. (Currently amended) The cluster resonator of claim 45, wherein the first and second conducting pads are external relative to the first and second conducting planes.

12. (Currently amended) The cluster resonator of claim 45 or 6, wherein its topology comprises a mechanically balanced structure.

13. (Currently amended) The cluster resonator of claim 45 or 6, wherein the first and second conducting planes are metallic layers incorporated with a multi-layered panel circuit.

14. (Previously presented) The cluster resonator of claim 13, wherein the multi-layered panel circuit is a multi-layered printed circuit board and the cluster resonator comprises an array of plated through holes.

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15. (Previously presented) The cluster resonator of claim 13, wherein the multi-layered panel circuit is a multi-chip module.

16. (Previously presented) The cluster resonator of claim 13, wherein the multi-layered panel circuit is a semiconductor chip.

17. (Currently amended) The cluster resonator of claim—35, wherein the cluster of vias is disposed along a circular path.

18. (Currently amended) The cluster resonator of claim—35, wherein the cluster of vias is disposed along an elliptical path.

19. (Currently amended) The cluster resonator of claim—35, wherein the cluster of vias is disposed along a polygonal path.

20. (Currently amended) The cluster resonator of claim—45, wherein spacing of vias within the cluster of vias effects a Faraday cage that substantially shields the interior region from RF fields propagating within the first and second conducting planes.

21. (Previously presented) The cluster resonator of claim 20, wherein spacing of the vias within the cluster of vias in relation to the interior vias effects a predetermined line impedance in the interior vias.

22. (Previously presented) A cluster resonator, comprising:  
a first conducting plane;  
a second substantially parallel conducting plane;

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a cluster of vias of essentially uniform length oriented substantially normal to the conducting planes, each via in the cluster comprising a first end and a second end;

first ends of each via in the cluster of vias coupled with the first conducting plane; and

a first conducting pad disposed in a third plane parallel and external to the region between the first and second conducting planes and capacitively coupled to the second conducting plane and physically coupled to each via in the cluster of vias proximate their second ends, wherein the vias in the cluster of vias are physically connected to only the first conducting plane and the first conducting pad.

23. (Previously presented) The cluster resonator of claim 22, wherein a combined inductance and capacitance of the cluster of vias form an electromagnetically resonant shunt circuit between the first and second conducting planes.

24. (Previously presented) The cluster resonator of claim 22, wherein the vias of the cluster of vias are disposed along a perimeter that defines an interior region.

25. (Original) The cluster resonator of claim 24, wherein one or more interior vias are routed within the interior region of the cluster of vias.

26. (Previously presented) The cluster resonator of claim 25, wherein the interior vias comprise portions of transmission lines passing electrical signals through the resonant element.

27. (Canceled)

28. (Canceled)

29. (Previously presented) The cluster resonator of claim 22 comprising a second cluster of vias, each via in the second cluster of vias comprising a first end and a second end, wherein the vias in the second cluster of vias are coupled proximate their first ends to the second conducting plane and proximate their second ends to a second conducting pad disposed in a fourth plane parallel and external to the region between the first and second conducting planes and capacitively coupled to the first conducting plane, wherein the vias in the cluster of vias are physically connected to only the second conducting plane and the second conducting pad.

30. (Canceled)

31. (Currently amended) The cluster resonator of ~~claims~~ claim 29 and ~~30~~, wherein its topology comprises a mechanically balanced structure.

32. (Previously presented) The cluster resonator of claim 22, wherein the first and second conducting planes are metallic layers incorporated with a multi-layered panel circuit.

33. (Previously presented) The cluster resonator of claim 32, wherein the multi-layered panel circuit is a multi-layered printed circuit board and the cluster resonator comprises an array of plated through holes.

34. (Previously presented) The cluster resonator of claim 22, wherein the multi-layered panel circuit is a multi-chip module.

35. (Previously presented) The cluster resonator of claim 22, wherein the multi-layered panel circuit is a semiconductor chip.

36. (Original) The cluster resonator of claim 24, wherein the cluster of vias is disposed along a circular path.

37. (Original) The cluster resonator of claim 24, wherein the cluster of vias is disposed along an elliptical path.

38. (Original) The cluster resonator of claim 24 wherein the cluster of vias is disposed along a polygonal path.

39. (Previously presented) The cluster resonator of claim 25, wherein spacing of the vias of the cluster of vias effects a Faraday cage that substantially shields the interior region from RF fields propagating within the first and second conducting planes.

40. (Previously presented) The cluster resonator of claim 39, wherein spacing of the vias of the cluster of vias in relation to the interior vias effects a predetermined line impedance in the interior vias.

41. (Canceled)

42. (Currently amended) The cluster resonator of ~~claim 4~~claims 5 or 6, further comprising a plurality of resonant vias and associated first and second conducting pads disposed in a periodic array associated with the first and second conducting planes.

43. (Previously presented) The cluster resonator of claim 22, further comprising a plurality of resonant vias and associated first conducting pads disposed in a periodic array associated with the first and second conducting planes.

44. (Currently amended) ~~An apparatus for suppressing electromagnetic interference~~A cluster resonator comprising:

a first conducting pad;

a second substantially parallel conducting pad; and

a cluster of vias of essentially uniform length disposed between and oriented substantially normal to the conducting pads, each via of the cluster of vias having a first end and a second end, wherein the first and second ends are physically connected respectively to the first and second conducting pads;

wherein the vias of the cluster of vias are disposed along a perimeter thereby forming a substantially field free interior region therewithin; and



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wherein one or more electrically isolated interior vias traverse the interior region of the cluster of vias, the interior vias comprising portions of transmission lines for passing electrical signals therethrough.

45. (Currently amended) The ~~apparatus~~cluster resonator of claim 44, wherein a spacing of the vias of the cluster of vias in relation to the interior vias is selected to effect a predetermined line impedance in the interior vias.

46. (Currently amended) The ~~apparatus~~cluster resonator of claim 44, wherein a diameter of the vias of the cluster of vias is selected to effect a predetermined inductance.

47 (Currently amended) The cluster resonator of ~~claim 4~~claims 5 or 6, wherein a diameter of the vias of the cluster of vias is selected to effect a predetermined inductance.

48. (Previously presented) The cluster resonator of claim 22, wherein a diameter of the vias of the cluster of vias is selected to effect a predetermined inductance.

49. (Currently amended) The ~~apparatus~~cluster resonator of claim 44, wherein the cluster of vias is disposed along a circular path.

50. (Currently amended) The ~~apparatus~~cluster resonator of claim 44, wherein the cluster of vias is disposed along an elliptical path.

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51. (Currently amended) The ~~apparatus~~cluster resonator of claim 44, wherein the cluster of vias is disposed along a polygonal path.

52. (Currently amended) The ~~apparatus~~cluster resonator of claim 44, wherein the first and second conducting pads are metallic layers incorporated within a multi-layered panel circuit.

53. (Currently amended) The ~~apparatus~~cluster resonator of claim 52, wherein the multi-layered panel circuit is a multi-layered printed circuit board and the cluster resonator comprises an array of plated through holes.

54. (Currently amended) The ~~apparatus~~cluster resonator of claim 52, wherein the multi-layered panel circuit is a multi-chip module.

55. (Currently amended) The ~~apparatus~~cluster resonator of claim 52, wherein the multi-layered panel circuit is a semiconductor chip.

56. (Currently amended) ~~An apparatus for suppressing electromagnetic radiation~~A cluster resonator comprising:

a first conducting plane;

a first substantially parallel conducting pad;

a cluster of vias oriented substantially normal to the first conducting plane and first conducting pad and disposed therebetween, each via of the cluster having a first end and a second end, wherein the first and second ends are physically connected respectively to the first conducting plane and first conducting pad;

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wherein the vias of the cluster of vias are disposed along a perimeter thereby forming a substantially field free interior region therewithin; and

wherein one or more electrically isolated interior vias traverse the interior region of the cluster of vias, the interior vias comprising portions of transmission lines for passing electrical signals therethrough.

57. (Currently amended) The ~~apparatus~~cluster resonator of claim 56, wherein a spacing of the vias of the cluster of vias in relation to the interior vias is selected to effect a predetermined line impedance in the interior vias.

58. (Currently amended) The ~~apparatus~~cluster resonator of claim 56, wherein a diameter of the vias of the cluster of vias is selected to effect a predetermined inductance.

59. (Currently amended) The ~~apparatus~~cluster resonator of claim 56, wherein the cluster of vias is disposed along a circular path.

60. (Currently amended) The ~~apparatus~~cluster resonator of claim 56, wherein the cluster of vias is disposed along an elliptical path.

61. (Currently amended) The ~~apparatus~~cluster resonator of claim 56, wherein the cluster of vias is disposed along a polygonal path.

62. (Currently amended) The ~~apparatus~~cluster resonator of claim 56, wherein the first conducting plane and first conducting pad are metallic layers incorporated within a multi-layered panel circuit.

63. (Currently amended) The ~~apparatus~~cluster resonator of claim 62, wherein the multi-layered panel circuit is a multi-layered printed circuit board and the cluster resonator comprises an array of plated through holes.

64. (Currently amended) The ~~apparatus~~cluster resonator of claim 62, wherein the multi-layered panel circuit is a multi-chip module.

65. (Currently amended) The ~~apparatus~~cluster resonator of claim 62, wherein the multi-layered panel circuit is a semiconductor chip.

66. (Currently amended) The ~~apparatus~~cluster resonator of claim 56, further comprising a second conducting plane substantially parallel to the first conducting plane wherein the first conducting pad is external to the region between the first and second conducting planes and capacitively coupled to the second conducting plane.

67. (Currently amended) The ~~apparatus~~cluster resonator of claim 56, further comprising a second conducting plane substantially parallel to the first conducting plane wherein the first conducting pad is internal to the region between the first and second conducting planes and capacitively coupled to the second conducting plane.

68. (Canceled)

69. (Currently amended) A cluster resonator comprising:  
a first conducting plane;  
a second substantially parallel conducting plane;

a first conducting pad disposed in a third substantially parallel plane internal to the region between the first and second conducting planes;

a first cluster of vias oriented substantially normal to the first conducting plane and first conducting pad and disposed therebetween, each via of the cluster having a first end and a second end, wherein the first and second ends are physically connected respectively to the first conducting plane and first conducting pad; and

a second conducting pad disposed in a fourth substantially parallel plane internal to the region between the first and second conducting planes;

a second cluster of vias oriented substantially normal to the second conducting plane and second conducting pad and disposed therebetween, each via of the cluster having a first end and a second end, wherein the first and second ends are physically connected respectively to the second conducting plane and second conducting pad; and

wherein the first and second conducting pads are proximate and capacitively coupled to each other; and

~~The cluster resonator of claim 68,~~ wherein the vias of the clusters of vias are disposed along a common perimeter thereby forming substantially field free interior regions therewithin; and

wherein one or more electrically isolated interior vias traverse the interior regions of the clusters of vias, the interior vias comprising portions of transmission lines for passing electrical signals therethrough.

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70. (Previously presented) The cluster resonator of claim 69, wherein a spacing of the vias of the clusters of vias in relation to the interior vias is selected to effect a predetermined line impedance in the interior vias.

71. (Previously presented) The cluster resonator of claim 69, wherein a diameter of the vias of the clusters of vias is selected to effect a predetermined inductance.

72. (Previously presented) The cluster resonator of claim 69, wherein the common perimeter is circular.

73. (Previously presented) The cluster resonator of claim 69, wherein the common perimeter is elliptical.

74. (Previously presented) The cluster resonator of claim 69, wherein the common perimeter is polygonal.

75. (Previously presented) The cluster resonator of claim 69, wherein the first and second conducting planes are metallic layers incorporated within a multi-layered panel circuit.

76. (Previously presented) The cluster resonator of claim 75, wherein the multi-layered panel circuit is a multi-layered printed circuit board and the cluster resonator comprises an array of plated through holes.

77. (Previously presented) The cluster resonator of claim 75, wherein the multi-layered panel circuit is a multi-chip module.

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78. (Previously presented) The cluster resonator of claim 75, wherein the multi-layered panel circuit is a semiconductor chip.